PATENT ABSTRACTS OF JAPAN

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(54) LOGICAL GATE CIRCUIT FOR SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PURPOSE: To select load capacity connected to the output line of a logical gate, altering an output load, and regulating the delay time of the logical gate by providing plural pieces of the load capacity through a switching circuit on a logical gate output side, and conductively controlling the switching circuit from the outside.
CONSTITUTION: Data inputted to an input terminal 1 are logical-operated by a logical gate 2, and outputted to an output terminal 3. The plural pieces of the load capacity by means of capacitors 7-1 to 7-m are connected through plural switching circuits 6-1 to 6-m to the output side of the logical gate 2. In addition, a decoding circuit 5 is connected to the switching circuits 6-1 to 6-m, the switching circuits 6-1 to 6-m are controlled by outputs b1 to bm of the circuit 5, and the load capacity is selected and altered. Further the outputs b1 to bm are outputted by the combination of the logical values of input pins a1 to am by the circuit 5, and by altering the capacity of the output load, the delay time of the logical gate 2 is regulated.